CLAIMS

What is claimed is:

1. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, the primary channel bank capable of providing clock synchronization to the secondary channel bank, wherein the primary channel bank and the secondary channel bank each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces; and

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces.

2. The system of claim 1, wherein the primary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the primary channel bank.

3. The system of claim 2, wherein the primary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the primary channel bank.

4. The system of claim 2, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

5. The system of claim 1, wherein the secondary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the secondary channel bank.

6. The system of claim 5, wherein the secondary channel bank further comprises a synchronous optical

network (SONET) framer connected to the STS cross-connect controller in the secondary channel bank.

7. The system of claim 5, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

8. The system of claim 1, wherein the TDM interface is capable of supporting 16 time division multiplexed channels.

9. The system of claim 1, wherein the ATM interface is capable of transporting 216 ATM cells per 125 μs frame.

10. The system of claim 1, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

11. The system of claim 1, wherein the primary channel bank further comprises a timing generator to provide timing reference to the TSI and ATM access controllers in the primary channel bank, the timing generator having a timing reference input and a clock

synchronization output connected to the secondary channel bank.

12. The system of claim 11, wherein the timing reference input comprises a synchronous optical network (SONET) timing reference input.

13. The system of claim 11, wherein the timing reference input comprises a T1 timing reference input.

14. The system of claim 11, wherein the timing reference input comprises a building integrated timing supply (BITS) input.

15. The system of claim 11, wherein the secondary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the secondary channel bank, the timing generator in the secondary channel bank synchronized by a clock synchronization signal received from the clock synchronization output of the primary channel bank.

16. The system of claim 1, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

17. The system of claim 16, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

18. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, the primary channel bank capable of providing clock synchronization to the secondary channel bank, wherein the primary channel bank and the secondary channel bank comprise respective node control processors capable of communicating to each other, each of the node control processors comprising:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces;

(iii) a synchronous transport signal (STS) cross-connect controller connected to the TSI; and

(iv) a synchronous optical network (SONET) framer connected to the STS cross-connect controller.

19. The system of claim 18, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

20. The system of claim 18, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

21. The system of claim 18, wherein the STS cross-connect controller is capable of supporting at least 12 STS-1 channels.

22. The system of claim 18, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

23. The system of claim 18, wherein the primary channel bank further comprises a timing generator to provide timing reference to the TSI and the ATM access controller in the primary channel bank, the timing generator having a timing reference input and a clock synchronization output connected to the secondary channel bank.

24. The system of claim 23, wherein the timing reference input comprises a synchronous optical network (SONET) timing reference input.

25. The system of claim 23, wherein the timing reference input comprises a T1 timing reference input.

26. The system of claim 23, wherein the timing reference input comprises a building integrated timing supply (BITS) input.

27. The system of claim 23, wherein the secondary channel bank further comprises a timing generator to provide timing reference to the TSI, the STS cross-connect controller and the ATM access controller in the secondary channel bank, the timing generator in the secondary channel bank synchronized by a clock synchronization signal received from the clock synchronization output of the primary channel bank.

28. The system of claim 18, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

29. The system of claim 28, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

30. The system of claim 18, wherein each of the node control processors further comprises a microprocessor connected to the TSI and the ATM access controller.

31. The system of claim 30, wherein each of the node control processors further comprises a data link and control tone card (DCT) connected to the microprocessor.

32. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) at least a first secondary channel bank connected to the primary channel bank through the ATM and TDM interfaces, wherein the primary channel bank and the secondary channel bank each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces; and

(iii) a timing generator to provide timing reference to the TSI and the ATM access controller, the timing generator in the primary channel bank having a timing reference input and a clock synchronization output connected to provide clock synchronization to the timing generator in the secondary channel bank.

33. The system of claim 32, wherein the primary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the primary channel bank.

34. The system of claim 33, wherein the primary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the primary channel bank.

35. The system of claim 33, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

36. The system of claim 32, wherein the secondary channel bank further comprises a synchronous transport signal (STS) cross-connect controller connected to the TSI in the secondary channel bank.

37. The system of claim 36, wherein the secondary channel bank further comprises a synchronous optical network (SONET) framer connected to the STS cross-connect controller in the secondary channel bank.

38. The system of claim 36, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the secondary channel bank.

39. The system of claim 32, wherein the TDM interface is capable of supporting 16 time division multiplexed channels.

40. The system of claim 32, wherein the ATM interface is capable of transporting 216 ATM cells per 125 μs frame.

41. The system of claim 32, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

42. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a synchronous optical network (SONET) timing reference input.

43. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a T1 timing reference input.

44. The system of claim 32, wherein the timing reference input of the timing generator in the primary channel bank comprises a building integrated timing supply (BITS) input.

45. The system of claim 32, further comprising a second secondary channel bank connected to the primary channel bank through the TDM and ATM interfaces.

46. The system of claim 45, wherein the second secondary channel bank is connected to the first secondary channel bank through the TDM and ATM interfaces.

47. A scalable digital loop carrier system capable of providing voice, video and data communications, the system comprising:

(a) a primary channel bank;

(b) an asynchronous transfer mode (ATM) interface connected to the primary channel bank;

(c) a time division multiplex (TDM) interface connected to the primary channel bank; and

(d) a plurality of secondary channel banks connected to the primary channel bank through the ATM and TDM interfaces, wherein the primary channel bank and the secondary channel banks comprise respective timing generators and respective node control processors,

wherein the timing generators are capable of providing clock signals for the respective channel banks, the timing generator in the primary channel bank having a timing reference input and a clock synchronization output connected to provide clock synchronization to the timing generators in the secondary channel banks, and

wherein the node control processors each comprise:

(i) a time slot cross-connect interchanger (TSI) having a plurality of subscriber bus interfaces;

(ii) an ATM access controller connected to the TSI, the ATM access controller having a plurality of ATM cell bus interfaces;

(iii) a synchronous transport signal (STS) cross-connect controller connected to the TSI; and

(iv) a synchronous optical network (SONET) framer connected to the STS cross-connect controller.

48. The system of claim 47, further comprising a plurality of STS transport cards connected to the STS cross-connect controller in the primary channel bank.

49. The system of claim 47, further comprising a plurality of STS transport cards connected to the STS

cross-connect controller in the secondary channel banks.

50. The system of claim 47, wherein the STS cross-connect controller is capable of supporting at least 12 STS-1 channels.

51. The system of claim 47, wherein the TDM interface is capable of providing a plurality of synchronous transport signal-one (STS-1) channels in a synchronous optical network (SONET) frame.

52. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a synchronous optical network (SONET) timing reference input.

53. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a T1 timing reference input.

54. The system of claim 47, wherein the timing reference input of the timing generator in the primary channel bank comprises a building integrated timing supply (BITS) input.

55. The system of claim 47, wherein each of the node control processors further comprises a microprocessor connected to the TSI and the ATM access controller.

56. The system of claim 55, wherein each of the node control processors further comprises a data link and control tone card (DCT) connected to the microprocessor.